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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/896,793	06/28/2001	Robert D. Bushey	10004829-1	8285

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EXAMINER	
SINGH, DALIP K	

ART UNIT	PAPER NUMBER
2676	7

DATE MAILED: 12/10/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

TS

Office Action Summary	Application No.	Applicant(s)	
	09/896,793	BUSHEY, ROBERT D.	
	Examiner	Art Unit	
	Dalip K Singh	2676	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 September 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____.
4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Response to Remarks

1. This Office Action is in response to applicant's amendment dated September 16, 2003 in response to PTO Office Action dated June 20, 2003.

2. This PTO Office Action **acknowledges** that the previous PTO Office Action dated June 20, 2003 in paragraph 2 on page 2 **shows the wrong secondary reference information** (U.S. Patent No. 5,861,893 to Sturgess) instead of what the Examiner intended to quote **(U.S. Patent No. 5,598,525 to Nally et al.) which is the correct secondary reference**.

3. This PTO Office Action shows the correct secondary reference which is U.S. Patent No. U.S. Patent No. 5,598,525 to Nally et al. and, **therefore this is a new non-final office action**.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claim(s) 1, 4, 5, 7-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 5,943,064 to Hong in view of U.S. Patent No. 5,598,525 to Nally et al.

a. Regarding claim 1, Hong **discloses** an apparatus and method for processing and displaying multiply types of graphics data for display comprising: a graphics pipeline (graphics processing engine and graphics display engine 50, Figure 3) and a bit map image pipeline (video display engine 44) including a plurality of stages (...the video display engine may also comprise a horizontal/vertical scaling and color space conversion means...col. 7, lines 65-67; col. 8, lines 1-17) configured to process a

bit-mapped image. However, Hong **does not disclose** a selectively configurable interconnection matrix defining an image path for providing selected outputs from one or more of said stages of one of said pipelines to selected inputs of one or more of said stages of the other of said pipelines. Nally et al. **discloses** a selectively configurable interconnection matrix defining an image path for providing selected outputs (...the graphics pseudo-pixels output from attribute controller 233...col. 10, lines 15-20) from one or more of said stages (...attribute controller 233 and the...graphics or video data output...from serializer 236...col. 10, lines 15-20) of one of said pipelines (...graphics back-end pipeline 205...includes attribute controller 233...col. 9, lines 25-29) to selected inputs of one or more of said stages (...are provided to the inputs of color comparison circuitry 302...col. 10, lines 15-20) of the other of said pipelines (...video back-end pipeline 204...col. 10, lines 4-15). Therefore, it would have been obvious to a person of ordinary skill in the art at the time invention was made to modify the graphics pipelines as taught by Hong with the "plurality of stages with ability to use selected outputs of one or more stages of said pipelines to selected inputs of one or more stages of said pipelines" as taught by Nally et al. **because** it provides for an efficient processing of graphics object data (...memory control circuitry controls...transfer of data between the first and second back-end pipelines...col. 3, lines 46-52...user is given total control of overlay options...col. 4, lines 23-35).

b. Regarding claim 4, Hong **discloses** an output stage connected to an output from each of said pipelines (...both the video display engine 26 and the graphics display engine 24 may transmit their pixel data...through common switching circuitry 28...col. 6, lines 20-28).

c. Regarding claim 5, Hong **does not disclose** providing selected outputs from one or more of said stages of one of said pipelines to selected inputs of one or more of

said stages of the other of said pipelines (...video back-end pipeline 204...col. 10, lines 4-15). Nally et al. **discloses** for providing selected outputs (...the graphics pseudo-pixels output from attribute controller 233...col. 10, lines 15-20) from one or more of said stages (...attribute controller 233 and the...graphics or video data output...from serializer 236...col. 10, lines 15-20) of one of said pipelines (...graphics back-end pipeline 205...includes attribute controller 233...col. 9, lines 25-29) to selected inputs of one or more of said stages (...are provided to the inputs of color comparison circuitry 302...col. 10, lines 15-20) of the other of said pipelines (...video back-end pipeline 204...col. 10, lines 4-15). However, it would have been obvious to a person of ordinary skill in the art at the time invention was made to modify the device as taught by Hong with the feature "routing outputs from one or more of plurality of stages to a next stage or to a selected one of plurality of stages such as graphics pipelines for 2D and 3D processing" as taught by Nally et al. **because** it provides for a flexible way to process data between the two pipelines.

d. Regarding claim 7, Hong **does not disclose** a data format converter configured to convert between a graphics data format and a bit-mapped image data format. Nally et al. **discloses** conversion circuitry allowing graphics data to be converted to a YUV format (col. 7, lines 45-57). However, it would have been obvious to a person of ordinary skill in the art at the time invention was made to modify the device as taught by Hong with Nally's "conversion circuitry" **because** it provides a means to flexibly process data in either graphics data or bit-mapped image data format.

e. Regarding claim 8, Nally et al. **discloses** encoding circuitry to identify and encode graphic images within said bit-mapped image (...video front-end pipeline 200 also includes encoding circuitry 214...which is then written into the video frame buffer space of frame buffer 105...col. 7, lines 45-50).

f. Regarding claim 9, Hong **discloses** routing of one of said graphic object and said bit-mapped image object between both said graphics and bit-mapped image pipelines (...in a first mode...generate a first type of graphics pixel data...second mode...video pixel data can be...captured...col. 3, lines 30-57; col. 4, lines 44-67).

g. Regarding claim 10, it is similar in scope to claim 1 above and is rejected under the same rationale.

h. Regarding claim 11, it is similar in scope to claim 2 above and is rejected under the same rationale.

i. Regarding claim 12, it is similar in scope to claim 3 above and is rejected under the same rationale.

j. Regarding claim 13, it is similar in scope to claim 4 above and is rejected under the same rationale.

k. Regarding claim 14, it is similar in scope to claim 5 above and is rejected under the same rationale.

l. Regarding claim 15, it is similar in scope to claim 6 above and is rejected under the same rationale.

a. Regarding claim 16, it is similar in scope to claim 7 above and is rejected under the same rationale.

m. Regarding claim 17, it is similar in scope to claim 8 above and is rejected under the same rationale.

n. Regarding claim 18, it is similar in scope to claim 9 above and is rejected under the same rationale.

o. Regarding claim 19, it is similar in scope to claim 4 above and is rejected under the same rationale.

p. Regarding claim 20, it is similar in scope to claims 2 and 3 above and is rejected under the same rationale.

6. Claim(s) 2, 3 and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 5,943,064 to Hong in view of U.S. Patent No. 5,598,525 to Nally et al. as applied to claim 1 above and further in view of U.S. Patent No. 5,861,893 to Sturgess.

a. Regarding claim 2, Hong-Nally combination although **disclose** graphics pipeline with conversion circuitry plurality of stages different from the others **but does not disclose** clipping, windowing to viewport, projection and sorting explicitly. Sturgess **discloses** a graphics controller that including graphics resources to accelerate selected processing steps in 2D and 3D pipelines (...geometry transformations, lighting calculations...col. 4, lines 25-60) and the selection from among the group of stages (...graphics commands that initiate and control these processing steps...are specified in a data structure called the execute buffer...col. 4, lines 48-52...3D graphics commands may specify...color space conversion...col. 7, lines 1-20). Therefore, it would have been obvious to a person of ordinary skill in the art at the time invention was made to modify Hong-Nally combination with the feature "geometry transformations using different processes including converting 3D coordinates to screen, lighting calculations" as taught by Sturgess **because** it provides for accelerated processing steps in graphics pipelines.

b. Regarding claim 3, Sturgess **discloses** wherein each of said second plurality of stages is different from the others (...2D pipeline block transfers data between memory locations...BLTs are processing steps in a 2D pipeline...hardware independence is accomplished through a device independent bitmap (DIB) engine 232...which provide...implementations for many of the processes in a typical 2D process pipeline...col. 3, lines 24-26; col. 5, lines 40-45) and the selection from among the group of stages (...2D commands may include ...color conversion...palette operations...col. 7,

lines 12-19). Therefore, it would have been obvious to a person of ordinary skill in the art at the time invention was made to modify Hong-Nally combination with the feature "color conversion, palette operations associated with 2D commands and processing" as taught by Sturgess **because** it provides parallel processing steps for 2D and 3D graphics pipelines resulting in efficient processing.

c. Regarding claim 6, Hong-Nally combination **does not disclose** wherein said graphics pipeline is configured to receive graphics data including graphics identification and location data and said bit-mapped image pipeline is configured to receive a raster scanned image data representing pixel luminance information. However, Sturgess **discloses** commands including a header that specifies a client (targeted resource), an opcode (function to be performed), and a data type (col. 6, lines 64-67; col. 7, lines 1-19). Therefore, it would have been obvious to a person of ordinary skill in the art at the time invention was made to modify Hong with the feature "header information, opcode and a data type" as taught by Sturgess **because** it provides for efficient data handling between the two pipelines.

Conclusion

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to **Dalip K. Singh** whose telephone number is **(703) 305-3895**. The examiner can normally be reached on Mon-Thu (8:00AM-6: 30PM) Fridays off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, **Matthew Bella**, can be reached at **(703) 308-6829**.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D.C. 20231

or faxed to:

(703) 872-9314 (for Technology Center 2600 only)

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA, Sixth Floor (Receptionist).

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Technology Center 2600 Customer Service Office whose telephone number is (703) 306-0377.

dks

December 3, 2003

Matthew C. Bella

MATTHEW C. BELLA
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